The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (**Currently Amended**) A method ~~for~~ **of** modifying electrical properties of a ~~multi-resistive state material~~ **two-terminal memory element in a cross point memory array,** comprising:

providing a substrate with active circuitry and multiple layers of conductive paths;

supplying a plurality of two-terminal memory elements between pairs of conductive array lines in a cross point array directly over the substrate, each two-terminal memory element comprising a praseodymium (Pr), calcium (Ca), manganese (Mn), and oxygen (O) perovskite as a multi-resistive state material;

doping the multi-resistive state material to modify at least one electrical property of the multi-resistive state material; **and**

~~**supplying the multi-resistive state material between a pair of electrodes; and**~~

applying at least one electrical pulse to the pair of ~~**electrodes**~~ **conductive array lines**, the electrical pulse having a selected polarity, a selected width, a selected maximum value and a selected waveform so as to create an electric field in the multi-resistive state material greater than a threshold electric field value to reversibly change the resistivity of the multi-resistive state material, the pulse having a pulse energy less than a pulse energy required to damage the multi-resistive state material.

2. (Original) The method of claim 1, wherein:

doping the multi-resistive state material modifies resistivity.

3. (Original) The method of claim 2, wherein:

the electrical pulse reversibly changes the resistivity of the multi-resistive state material to a value between 0.1 Ω-cm and 1.0 Ω-cm.

4. (Original) The method of claim 1, wherein:

doping the multi-resistive state material modifies the amount of charge traps.

5. (Original) The method of claim 1, wherein:

doping the multi-resistive state materials improves the data retention capability of the multi-resistive state material.

6. (**Currently Amended**) The method of claim 1, wherein:

~~**the**~~ **an** interface between the ~~**electrodes**~~ **pair of conductive array lines** and the multi-resistive state material causes an ohmic effect.

7. (**Currently Amended**) The method of claim 1, wherein:

~~**the**~~ **an** interface between the ~~**electrodes**~~ **pair of conductive array lines** and the multi-resistive state material causes a Schottky effect.

8. (Original) The method of claim 1, wherein:

the electrical pulse reversibly changes the resistivity of the multi-resistive state material from either a high value to a low value or from a low value to a high value; and

doping the multi-resistive state material modifies the magnitude of the difference from the high value to the low value.

9. (**Currently Amended**) The method of claim 8, wherein:

~~**the**~~ **an** interface between the ~~**electrodes**~~ **pair of conductive array lines** and the multi-resistive state material causes an ohmic effect.

10. **(Currently Amended)** The method of claim 8, wherein:

~~the~~ an interface between the ~~electrodes~~ pair of conductive array lines and the multi-resistive state material causes a Schottky effect.

11. (Original) The method of claim 1, wherein:

the electrical pulse reversibly changes the resistivity of the multi-resistive state material to a value between 0.1 Ω-cm and 1.0 Ω-cm.

12. (Original) The method of claim 1, wherein:

doping the multi-resistive state material causes the multi-resistive state material's electrical properties to be more uniform, whereby the electrical properties of the multi-resistive state material have a greater predictability.

13. (Original) The method of claim 1, wherein:

doping the multi-resistive state material additionally reduces the temperature sensitivity of the multi-resistive state material's resistance.

14. **(Currently Amended)** The method of claim 4, wherein:

~~the~~ an interface between the ~~electrodes~~ pair of conductive array lines and the multi-resistive state material causes an ohmic effect.

15. **(Currently Amended)** The method of claim 4, wherein:

~~the~~ an interface between the ~~electrodes~~ pair of conductive array lines and the multi-resistive state material causes a Schottky effect.

16 - 18. **(Canceled)**

19. (Original) The method of claim 1, wherein:

doping the multi-resistive state material reduces magnetic field dependence.

20. (Original) The method of claim 1, wherein:

the selected waveform is either a square, saw-toothed, triangular, sine wave, or some combination thereof.

21. (Original) The method of claim 1, wherein:

the selected maximum value of the selected waveform is between 1 volt and 15 volts.

22. (Original) The method of claim 1, wherein:

the selected waveform has a duration between 1 nanosecond and 100 microseconds.

23. (Original) The method of claim 1, wherein:

at least two electrical pulses are applied to the multi-resistive state material in order to reversibly change its resistivity.

24. (Original) The method of claim 1, wherein:

the electrical pulse reversibly changes the resistivity of the multi-resistive state material from either a high value to a low value or from a low value to a high value; and

once the multi-resistive state material's resistivity is changed, application of an opposite polarity second electrical pulse will cause the multi-resistive state material's resistivity to revert back to a low value if it was changed to high, or a high value if it was changed to low.

25. (Original) The method of claim 1, further comprising:

doping the multi-resistive state material with a second dopant to modify another electrical property of the multi-resistive state material.

26. **(Withdrawn)** A memory comprising:

an array of memory cells, each memory cell including a memory element; and

selection circuitry that is capable of selecting a single memory cell or a group of memory cells out of the array of memory cells;

wherein each memory cell exhibits a hysteresis that is characterized by a first write threshold when the memory cell is in a low resistive state and a second write threshold when the memory cell is in a high resistive state such that

voltages applied across the memory cell that are higher than the first write threshold have substantially no effect on the resistive state of the memory cell when the memory cell is in the low resistive state; and

voltages applied across the memory cell that are lower than the second write threshold voltage have substantially no effect on the resistive state of the memory cell when the memory cell is in the high resistive state; and

wherein the structure of the memory element is intentionally modified to improve some memory characteristics of the memory cell.

27. **(Withdrawn)** The memory of claim 26, wherein:

the memory element has a crystalline matrix that is made of atoms; and

the structure of the memory element is intentionally modified by substituting atoms within the crystalline matrix with a dopant.

28. **(Withdrawn)** The memory of claim 26, wherein:

the memory element has a crystalline matrix; and

the structure of the memory element is intentionally modified by interstitially introducing a dopant into a crystalline matrix.

29. **(Withdrawn)** The memory of claim 26, wherein:

the memory element has a crystalline matrix; and

the structure of the memory element is intentionally modified by growing the memory element on a seed layer that has a crystalline matrix that is dissimilar from the crystalline matrix of the memory element.

30. **(Withdrawn)** The memory of claim 26, wherein:

the memory element has an amorphous structure.